REMARKS

Claims 1-8 are currently pending in this application.

The Examiner has objected to the Abstract. Applicants have amended the Abstract herein and attach herewith a copy of the Abstract on a separate page. The specification has been reviewed and minor typographical errors are corrected herein. No new matter has been added. Entry of these amendments is respectfully requested.

Claims 1-4 and 6 stand objected to because of certain minor informalities involving a lack of antecedent basis for certain terms. Claims 1-4 and 6 have been amended herein to address those informalities and are now deemed to be in condition for allowance. A minor grammatical amendment has also been made to claims 1-8 by insert --an-- before "electronic" in line 1 thereof. The title has also been amended in the same manner.

Claims 1, 7 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,990,546 to Igarashi et al. (Igarashi). Claims 1, 7 and 8 also stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,821,627 to Mori et al. (Mori).

Claim 1 of Igarashi discloses a semiconductor device comprising a semiconductor chip having an electrode; a first insulating layer facing said semiconductor chip; a second insulating layer laminated on said first insulating layer; an inner electrode fixed on said first insulating layer, said inner electrode being connected to said electrode of said semiconductor chip; an outer electrode fixed on said second insulating layer, said outer electrode being connected to a conductor end of a circuit board; a routine conductor bridging said inner and outer electrode, said routing conductor being sandwiched by said first and second insulating layers; and resin sealing the space between said semiconductor chip and said first insulating layer.

Igarashi also describes that the inner electrode 21 thus formed after filling the hole 212 with metal, metallic bumps 211 each having a height of 10 to 150 μm are formed on the filling metals 213, which may include gold, silver, nickel, copper, palladium, etc. See column 5, lines 49-54 of Igarashi.

Mori discloses an electronic circuit device comprising a substrate; a wiring layer formed on a surface of said substrate; bump-like bonding means formed on said wiring layer; a barrier metal layer formed on said bonding means; and a micro electronic element formed on said barrier metal layer, see claim 1 of Mori.

Mori also describes that as shown in Fig. 16A, as a barrier metal B, a titanium layer, a nickel layer, and a palladium layer are formed on the bonding pad of the semiconductor element from the semiconductor element side, and the resultant structure is electroplated to obtain the gold bumps 12. In this case, the titanium layer is formed to increase the adhesion strength with the aluminum pad, the nickel layer is formed to prevent diffusion of gold into the bonding pad of the semiconductor element, and the palladium layer is formed to increase the bonding strength with the gold. See column 17, lines 15-24 of Mori.

The present invention, on the other hand, as defined in claim 1, requires a film carrier tape for mounting an electronic part, which comprises an insulating film and a wiring pattern made of a conductive metal and provided on a surface of the insulating film, wherein an undercoating layer containing nickel as a main constituent is formed on at least a part of a surface of the wiring pattern made of a conductive metal, an intermediate layer containing palladium as a main constituent is formed on a surface of the undercoating layer, a surface layer containing gold as a main constituent is formed on a surface of the palladium-containing intermediate layer. The average thickness of the intermediate layer containing palladium as a main constituent is not more than about 0.04 μm.

It is clear that Igarashi and Mori do not teach or suggest a distinct three-layer structure of nickel, palladium and gold containing materials as required in claim 1 of the present application.

Moreover, Igarashi and Mori do not teach or suggest a thickness of an intermediate palladium layer as being no more than about 0.04 μm as specified in claim 1 of the present application.

As exemplified in Examples 1 to 3 of the specification, a film carrier tape for mounting an electronic part having a three-layer structure of nickel, palladium and gold containing materials on at least a part of a surface of the wiring pattern as well as having a palladium plating thickness of no more than about 0.04

μm, i.e., 0.004 μm, 0.002 μm and 0.01 μm, respectively, as defined in claim 1 shows higher wire bonding strength, as well as a more narrow variability range of wire bonding strength and solder ball peel strength as compared to a corresponding one having no palladium plating layer, see Comparative Examples 1-3 and Tables 2-4 of the present application.

It is an object of the present invention to provide a film carrier tape for mounting an electronic part having high wire bonding strength, narrow variability of strength levels, high bonding reliability, and high connection stability of the solder ball disposed on the ball pad. See page 7, lines 16-20 of the instant specification.

The present invention does not involve routine optimization within the level of ordinary skill in the art as opined by the Examiner, but, rather, possesses novel features that produce a new and unexpected result over the prior art. Claim 1 is not taught or suggested by Igarashi or Mori taken alone or in combination and, thus, is not obvious. Claims 2-8 depend from claim 1 and, likewise, represent a patentable advance over the prior art of record because they depend from a patentable base claim.

Based on the foregoing amendments and remarks, reconsideration of the rejections and allowance of pending claims 1-8 are respectfully requested.

Respectfully submitted,

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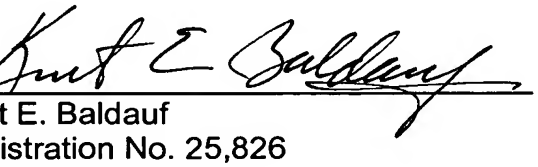
By 

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